Fabrication technology development of thin film transistors optimized with respect to the structure of the silicon films that results from the crystallization process

Despina C Moschou*

National and Kapodistrian University of Athens,
Department of Informatics and Telecommunications
dmoschou@imel.demokritos.gr

Abstract. The object of this dissertation was the electrical characterization of polycrystalline Si TFTs, crystallized with different variations of the advanced technique SLS ELA, and the determination of process technological parameters that affect the device performance. We began studying the TFT active region film microstructure, relating the film characteristics with the electrical performance of the TFTs. Then, we examined the relationship between critical process steps and TFT electrical characteristics. We also studied the role of the topology on TFT performance. Finally, we tried to modify the typical TFT fabrication procedure, studying the use of alternative gate dielectrics.

Key words: Polycrystalline Silicon, crystallization techniques, electrical characterization, process optimization

1 Introduction

The rapid technological progress of the last decades has brought huge changes in the everyday life of people worldwide. In particular, the microelectronics revolution has made several electronic equipment (personal computers, mobile phones, consumer electronics etc.) necessary for the function of modern societies. But as research advances, more and more microelectronic applications emerge. One such field are the so called large area electronics or macroelectronics [1], where the integrated circuits are not restrained on Si chips but can be placed on any substrate of any possible dimension [2]. The first and most typical example of such applications, which has conquered the global markets in recent years, are the flat panel displays[3]. However, in order to develop more and higher-performance large area electronics, it is essential to develop and optimize the cornerstone of this technology: the thin film transistor (TFT)[4]. Several reasearcher have been interested in that topic, each one focusing on a different kind of TFT: amorphous

* Dissertation Advisors: Angela Arapoyanni, Assoc. Professor and Dimitrios Kouvatsos, Main Researcher

Si TFTs [5], CdS TFTs [6], organic TFTs [7] or polycrystalline Si (poly-Si) TFTs [8], with each one featuring specific advantages and disadvantages

In this work we discuss poly-Si TFTs, due to their increased performance characteristics compared to their alternatives. That is why they are the ones considered by contemporary industries as the most promising for highly demanding applications. In particular, we deal with low temperature polycrystalline Si (LTPS) TFTs, which could be compatible with a broader range of substrate materials (such as plain glass or polymer), and therefore be applicable for more demanding applications. The low temperature crystallization process studied in this dissertation is the state of the art Sequential Lateral Solidification Excimer Laser Anneal (SLS ELA) [9], a technique little studied until now, yielding extremely high performance TFTs. The scope of the present dissertation was the fabrication technology development of such high performance TFTs and the determination of ways to optimize the procedure, in respect to TFT characteristics.

We began studying the effect of the TFT active region poly-Si film microstructure, relating it with the TFT electrical characteristics. Then, we examined the relationship between critical process steps-namely gate dielectric deposition, doping and activation and the channel dimensions to be selected-and TFT electrical parameters. We also studied the role of the topology (top gate, bottom gate, double gate) on TFT performance. Finally, attempting to further optimize the fabrication process of LTPS TFTs, we experimented with possible modifications of the typical fabrication process, studying the use of alternative gate dielectrics.

2 Results and Discussion

We began our work by studying the effect of the most important fabrication step for LTPS TFTs: the crystallization technique. We found a new electrical parameter: the difference of gate voltage for maximum transconductance ($V_{g,max}$) minus the threshold voltage (V_{th}) of the device, which can easily be calculated graphically (Fig. 1) through the I_{ds}-V_{gs} curves. We proved mathematically that this parameter ($V_{g,max}$-V_{th}) is proportional to the traps within the polycrystalline Si film, mainly to those of them that are located near the edges of the bandgap ($N_t^{band-edge}$). This electrical parameter is not affected by other techological factors that influence the already known and used electrical parameters (V_{th}, S, $G_{m,max}$).

Proceeding, we compared the oldest and most understood Si crystallization method, Solid Phase Crystallization (SPC), with the advanced SLS ELA technique, probing the points and causes that make the SLS ELA poly-Si TFTs be far superior than the SPC crystallized. As we expected, the SPC sample features an almost three times larger polysilicon trap density, the quality of the poly-Si/SiO_2 is much worse, while the quality of the grain itself is also much lower. All these microstructural characteristics of SPC poly-Si affect the very low field effect mobility μ observed, compared always to the SLS ELA sample,

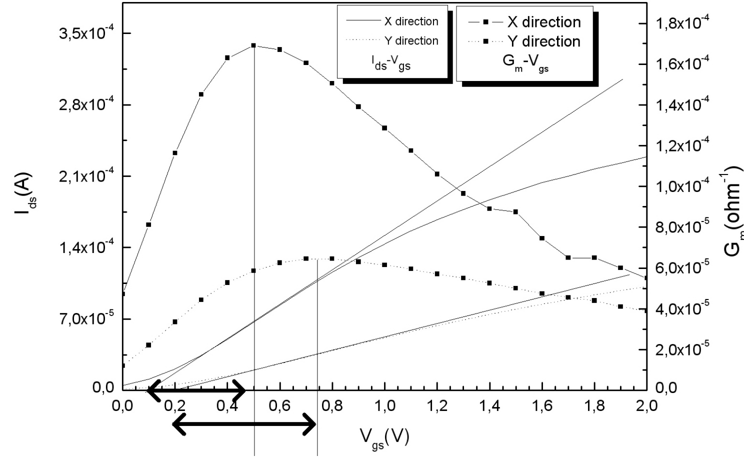

Fig. 1. Graphical calculation of $V_{g,max}$-V_{th} parameter for one preferentially oriented LTPS TFT and one non-preferentially oriented.

but at the same time its very intense sensitivity to dc stress (Fig. 2). Moreoever, they can explain the observed differences in degradation mechanisms.

Having confirmed the clear superiority of SLS ELA films, in the rest of our work we focus only in these. We further investigated the polysilicon film itself, as this results from each SLS ELA technique utilized, before any transistors are fabricated in it. We characterized several advanced SLS ELA films morphologically (SEM, AFM) and optically (UV-visible spectroscopy, spectroscopic ellipsometry, XRD analysis), in order to gather detailed information on their microstructure. The XRD data (Fig. 3)revealed that the different SLS ELA techniques give a material significantly differentiated, as far as crystallinity is concerned, from amorphous and crystalline Si, probably due to its special crystalline structure, resembling that of allo-Si. This Si crystal modification is a structure similar to graphene and consists of lamellar crystals. Therefore, the special characteristics observed in these films could be attributed to the atom arrangement itself. Moreover, we probed for the first time a possible analogy between an optical parameter (E_d: the material dispersion energy according to the Wemple-DiDomenico single oscillator model) and an electrical parameter ($V_{g,max}$-V_{th}) of the films.

We proceeded with the electrical characterization of TFTs fabricated in SLS ELA films, in order to see the film microstructure effect on the device electrical performance. We began by studying the effect of grain boundaries on our transistors. We characterized TFTs fabricated with different crystallization techniques, the only difference being the channel orientation in respect to the film grain boundaries. We saw that the effect of each technique on film directionality is different. Next, we compared different SLS ELA crystallization techniques, with the TFT channels always oriented in the preferential direction of each technique, so as to locate the microstructure effect on TFT electrical performance. We con-

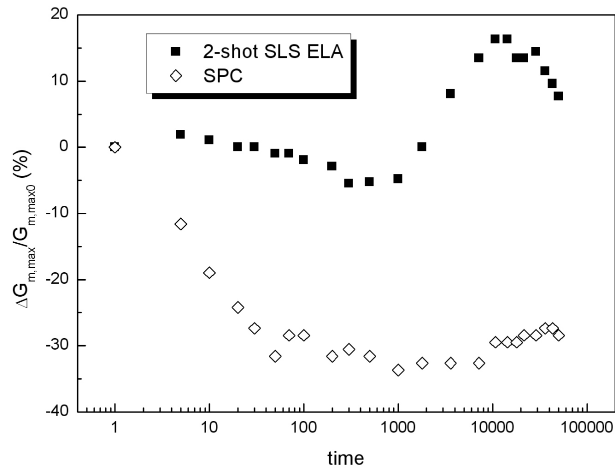

Fig. 2. Evolution of transconductance $G_{m,max}$ for an SPC and an SLS ELA TFT with dc stress time.

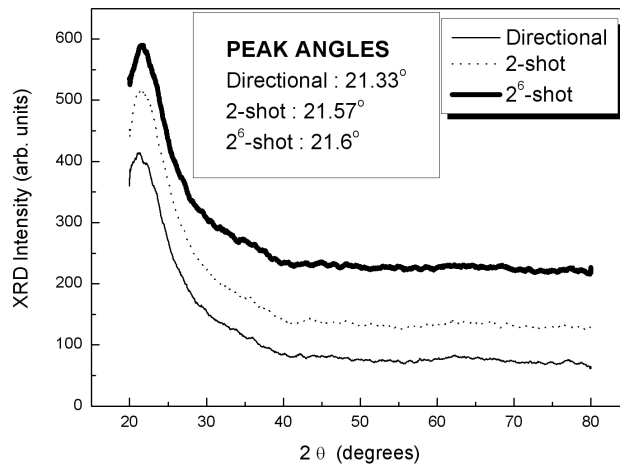

Fig. 3. XRD spectra of the three SLS ELA films examined.

cluded that an increased mobility μ is a combination of good poly-Si film quality and also low surface roughness, while at the same time the degradation mechanisms of SLS ELA TFTs (Fig. 4) depend, apart from the operation conditions, on the specific poly-Si film microstructure (roughness, intragrain quality, grain boundaries, grain size). Therefore, for each SLS ELA technique TFTs, optimum operation conditions should be employed.

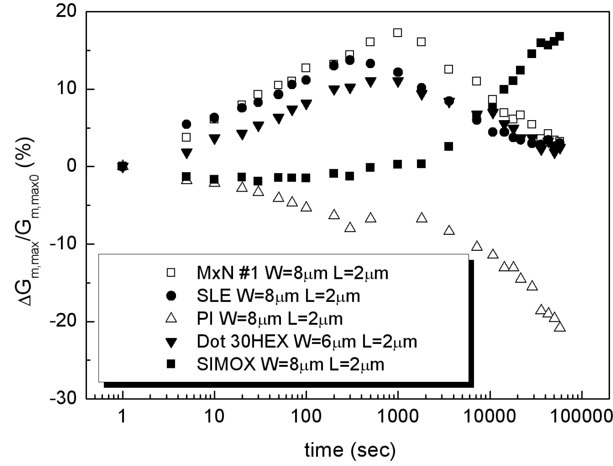

Fig. 4. Evolution of transconductance $G_{m,max}$ with dc stress time for SLS ELA TFTs crystallized with different techniques.

However, apart from the crystallization technique employed, significant importance in the operation of TFTs bear the rest of the fabrication steps, in which the typical fabrication process of MOSFETs is differentiated due to the low temperature constraints required. We, therefore, studied the gate dielectric deposition method effect on SLS ELA TFT electrical characteristics and reliability. We tried two techniques: PECVD and TEOS LPCVD. The latter yielded higher performance devices but with lower reliability. We also, investigated the role of doping for the development of n- and p- channel SLS ELA TFTs, characterizing both n- and p- devices crystallized by different SLS ELA techniques. It was found that a p- type doping could give lower trap density within the film and smaller electrical effect of the grain boundaries (Fig. 5). This effect was attributed to a slightly larger grain size after a p- type doping and to the absence of doping segregation in them.

Another important technological parameter that should always be considered for TFT fabrication is the geometrical dimensions of the devices, since it is known that they affect their electrical characteristics. We studied the impact of channel width W reduction and concluded that the effect of degraded channel edges (due to etching, doping etc.) could degrade the small channel width TFT

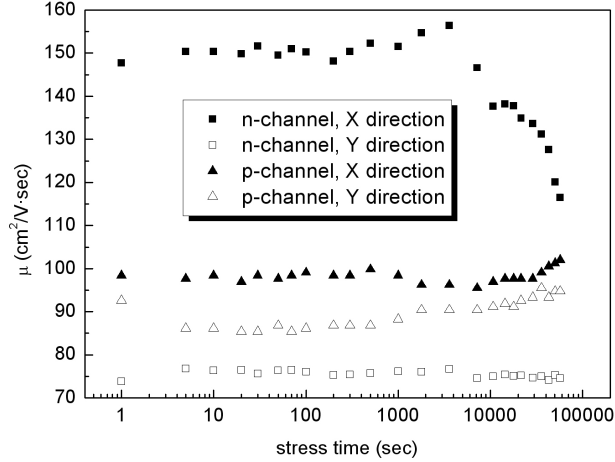

Fig. 5. Field effect mobility μ evolution with stress time for n- and p- channel TFTs, oriented both preferentially and non-preferentially.

performance further than expected. However, the channel length L effects proved more complicated. Two competitive mechanisms were observed: one reducing μ with diminishing L (for $L \leq L_{optimum}$) and one increasing μ with diminishing L (for $L \geq L_{optimum}$), which define an optimum channel length $L_{optimum}$ (Fig. 6). The use of this $L_{optimum}$ in the fabrication procedure could help obtain the best possible electrical performance for a given crystallization technique.

Moreover, since an appropriate device topology should be selected to fabricate a TFT, we characterized single gate trasistors, with the gate placed either at the top of the poly-Si film or at the bottom. It was observed that the yield for bottom gate topologies will be much lower than that of top gate topologies, if the bottom oxide thickness is not comparable to bottom gate poly-Si thickness. Also, the bottom interface will feature larger trap density than the top one (Fig. 7) because of the SLS ELA procedure, increasing the thermal budget on the underlying structure, and the recrystallization of poly-Si film. Therefore, the characteristics of bottom gate structures will always be worse than top gate ones, for such crystallization techniques.

We also studied a more complex topology: the double gate structure, featuring a top gate at the top surface of the poly-Si film and a bottom gate at the bottom one at the same time. The electrical parameters of double gate SLS ELA TFTs, with the poly-Si film being fully depleted, seemed to be adjustable at will by appropriately biasing the bottom gate. What is more, with the use of a physical model we developed, we can calculate the interface and oxide trap densities in double gate devices with asymmetrical gate lengths, for the first time. For the development of this model we assumed that a double gate transistor with larger top gate length L_t than bottom one L_b, can be modeled by a series connection of a) a double gate transistor with same top and bottom gate lengths

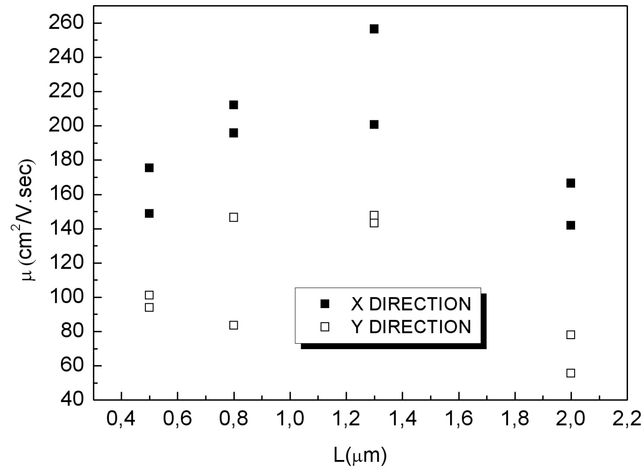

Fig. 6. Field effect mobility μ as a function of channel length L for n- channel SLS ELA TFTs of both orientations.

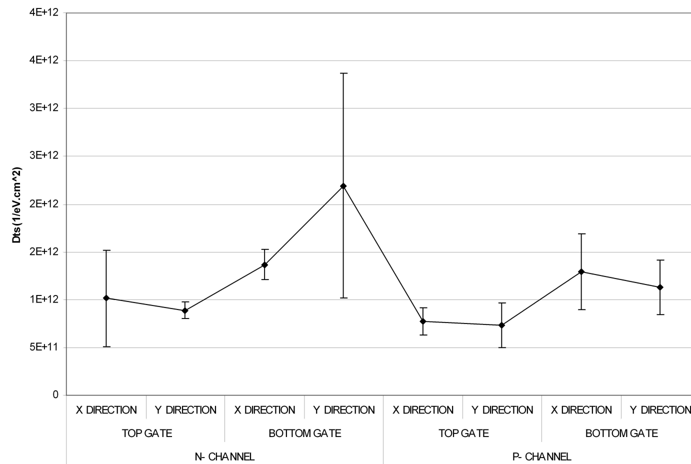

Fig. 7. Average trap density D_{ts} for top and bottom gate SLS ELA TFTs.

(L_t=L_b) and b) a top gate transistor with channel length L=L_t-L_b (Fig. 8). We applied this model to experimental data obtained by devices not optimized for this task. These initial tests showed that applying this model we were able to obtain quantitative results of the interface and oxide trap densities, for the first time. However, a more detailed investigation of the model limits and precision is still required, applying it to TFTs optimized for such work.

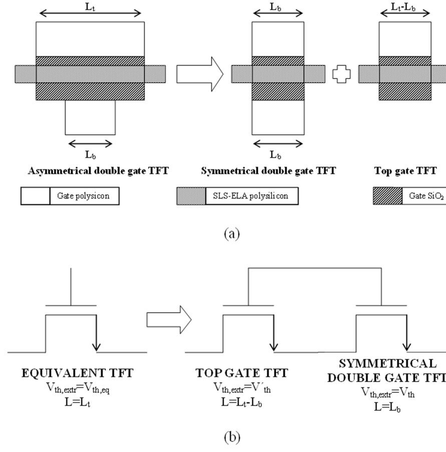

Fig. 8. Schematic of asymmetrical double gate device (a) and equivalent model (b) of our approach.

Finally, we proceeded to the development of LTPS TFTs with variations in their typical process flow. In particular we tried alternative dielectrics as gate insulators. We investigated the high-k dielectric HfO_2 for the first time in our laboratory. We obtained, after long fabrication tests, the optimum deposition and post-treatment conditions. At first, we were able to fabricate operational capacitors with HfO_2 as gate oxide and cocluded that the ideal gate electrode for them was Al. Nonetheless, because of the extremely high temperatures required, relatively to the SLS ELA temperature limits, W should be prefered for such applications. Poly-Si, due to its low adhesion on this dielectric and the unaccaptably low device reliability, can not be utilized (Fig. 9). In a final attempt, we tried to fabricate LTPS TFTs replacing the gate dielectric with HfO_2 and SiO_xN_y. Unfortunately this forst fabrication attempt did not yield operational devices.

3 Conclusions

Low temperature polycrystalline silicon thin film transistors are essential for large area electronics and high performance flat panel displays. In recent years,

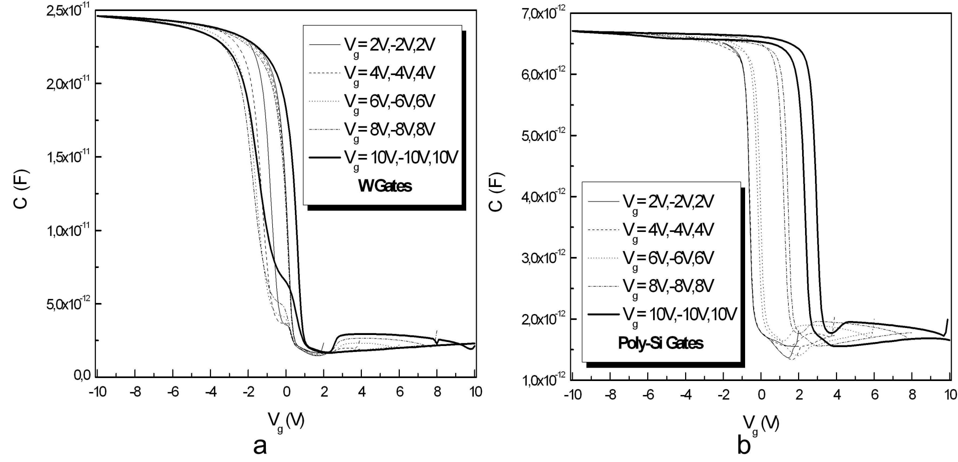

Fig. 9. Capacitance-voltage characteristics for capacitors with HfO_2 as gate dielectric and a)W gates, b)poly-Si gates

LTPS TFT performance has substantially increased due to important breakthroughs in the field of polycrystalline silicon crystallization and also due to the optimization of the process steps that differ from those of typical MOSFETs, mainly because of the requirement for low temperature procedures. The object of the present dissertation was the electrical characterization of polycrystalline Silicon thin film transistors, crystallized with different variations of the advanced technique SLS ELA, and the determination of process technological parameters that affect the device performance, in order to further optimize the production of such high performance transistors.

We began studying the effect of the TFT active region film microstructure, relating the film characteristics themselves with the electrical performance and reliability characteristics of the TFTs. We found a new electrical characterization parameter ($V_{g,max}$-V_{th}), offering new insight on poly-Si trap density. We verified and probed the reasons for the superiority of the SLS ELA crystallization technique compared to SPC. Through optical and morphological characterization we located a possible special atomic arrangment in such films. Electrical characterization of TFTs crystallized with different SLS ELA techniques revealed specific relationships between microstructural characteristics and electrical ones.

Then, we examined the relationship between critical process steps and SLS ELA TFT performance. We found that the method of gate dielectric deposition significantly affects the TFT electrical parameters and also their degradation mechanisms. We also concluded that the doping and activation procedures could optimize the fabrication procedure, since a p- type doping could yield films with lower grain boundary trap densities. Channel dimensions should carefully be selected, since there are specific, technology related narrow width and short channel mechanisms.

We also studied the role of the topology (top gate, bottom gate, double gate) on TFT performance. We saw that bottom gate structures are more likely to fail, due to the crystallization technique and the thickness of the films utilized. Even if they are operational, they will feature larger trap densities, due to the aforementioned reasons. A physically based model was developed for a double gate TFT with smaller bottom gate length than top one. The application of this model could give quantitative estimations of the oxide charge and interface trap densities.

Finally, we tried to modify the typical TFT fabrication procedure, studying the use of alternative gate dielectrics. We focused on the high-k dielectric HfO_2, fabricated capacitors using this material and studied possible, low temperature compatible gate electrodes. We concluded that the best possible gate electrode material to be used for LTPS HfO_2 TFT is W.

To sum up, through this work we extracted new characterization methodologies and new relationships between electrical and technological characteristics of high performance LTPS TFTs, while at the same time suggesting specific optimization points for all of the critical steps in the fabrication procedure. Therefore, this dissertation is a useful tool-guide for an optimized fabrication procedure of high performance LTPS TFTs.

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