

**CV of Constantin (Costas) Halatsis ([click here for greek](#))
Emeritus Professor of University of Athens, GR**



Contact:

Tel.: (+ 30) 210 7275201 (work) +(30) 210 6209908 (Home) +(30) 6976758964 (mobile)

Fax: (+ 30) 210 7275201

E-mail: halatsis@di.uoa.gr

URL: <http://www.di.uoa.gr/~halatsis>

Personal data

Academic lectures

Projects participated in

Publications

Synopsis

Constantin (Costas) Halatsis was born in Athens, Greece, in 1941. He received his B.Sc. degree in Physics in 1964 and his M.Sc. degree in Electronics in 1966, both from the University of Athens. In 1971 he received his Ph.D. degree in Computer Science from the University of Manchester, UK. From 1971 to 1981 it worked as researcher in the Centre of Computers of NCSR Demokritos, Greece, from where he retired as the Director of the Centre. In 1981 were elected Full Professor in the chair of Computers of the Department of Physics of the Aristotle University of Thessaloniki and in 1988 he was invited as Full professor in the Department of Physics University Athens. A year later he moved to the newly established Department of Informatics of the University of Athens, which in the year 2000 the Department was renamed as Department of Informatics and Telecommunications (see <http://www.di.uoa.gr>). Professor Halatsis served the Department until August 2008, and since then he is an Emeritus Professor of the Department. Recently, Professor Halatsis has been with the Neapolis University Pafos of Cyprus in setting up a School of Information Sciences for offering BSc and MSc studies respectively in the fields of Applied Informatics and Information Systems (see <http://www.nup.ac.cy>). Currently, he is a free lancer consultant of Informatics. For the five-years period 1988-93 he served, after election, as the Director of the Institute of Informatics and Telecommunications of the NCSR Demokritos. Also at intervals and for three years in total he worked as visiting Scientific Associate in the Data Handling Division of the European Organization for Nuclear Research CERN in Geneva, Switzerland, where he designed and built advanced hardware processors and innovative Software. Also, during the academic year 2007-08 he has been visiting Professor in the University of Cyprus and the Open University of Cyprus. Prof. Halatsis has taught a large number of different courses at the undergraduate and postgraduate levels and it has supervised the doctoral thesis of many students, some of which are today Professors in Greek Universities. It has been financed for several European and national research programs and he has compiled and publishes in international journals and conference proceeding more than 150 technical papers after peer review and he has enjoyed international recognition. His main research area is that of Computer Architecture, both at the single processor level and that of multiprocessor systems (Von Neumann and non Von Neumann types of Architecture) for high performance computing and networking, HPCN. He has conducted research in several other areas of CS, the main of which are in the areas of Artificial Intelligence (Logic Programming, Constraints Logic Programming, CLP), Software Eng, e-

government, e-learning (affective computing). His recent personal research activity is focused in fundamental open theoretical problems in Computer Science, continuing at the same time research on previous subjects. In the R&D side his recent activity is focused in the use of Virtual Reality for Cultural applications and on issues of Electronic Governance, e-gov, eID and Data Warehouse for the Cyprus Government.. Prof. Halatsis has served at various academic positions, he has participated in a number of international and national committees and councils, and he has served as member in many international and national evaluation committees for academic positions and R&D proposals. He has studied and designed large projects of national and international Information Systems and has contributed decisively in the growth and operation of the Faculty of Science and Technology of the University of Peloponnese, GR.

Detailed CV

Personal data

Name: Constantin (Costas) Halatsis

Title: Emeritus Professor of Computer Science, University of Athens, GR

Marital status: Married, two daughters, one grandson and two grandchildren

Studies

- 1964: B.Sc. in Physics, University of Athens, GR
- 1966: M.Sc. in Electronic, University of Athens, GR
- 1971: Ph.D. in Computer Science, University of Manchester (UMIST), UK.

Professional Qualifications

- 9/2008 - Today Emeritus Professor, Dept. of Informatics and Telecommunications, Univ. of Athens, GR
- 7/2017 – Today : Free Lancer Consultant
- 9/2014 - 6/2017: Professor of Informatics, Neapolis University Pafos, Cyprus
- 9/2009 – 8/2013: Consultant to Cyprus Government, the Department of Information Systems on e-Governance issues (government gateway, electronic identification, eID and Data Warehouse-Data Mining)
- 9/2009 – 6/2012 Teaching at Open University of Cyprus
- 9/1988 – 8/2008 Full professor of CS at the University of Athens, Department of Informatics and Telecommunications, GR
- 9/2007-8/2009 Visiting Professor at the University of Cyprus and the Open University of Cyprus
- 1988 - 1993 Director of the Institute of Informatics and Telecommunications of NCSR Demokritos, Athens, GR (in parallel with the position at the University of Athens)
- 1981 - 1988 Full professor of CS at the Aristotle University of Thessaloniki, GR
- 1985 - 1987 and 1978 - 1979 Scientific Associate of Data Handling Division CERN, Geneva, CH
- 1979 - 1981 Director of the Computer Centre of NCSR Demokritos, Athens, GR
- 1971 - 1979 Research Scientist at the Computer Centre of NCSR Demokritos, Athens, GR

Academic and Administrative positions served

- **Dean** of Faculty of Sciences in the Aristotle University of Thessaloniki, GR
- **Chairman of Department** in the University of Athens and in the University of Peloponnese, GR
- **Member of Senate** of the University of Athens and of the Aristotle University of Thessaloniki, GR.

- **Director** of the Institute of Informatics and Telecommunications, NCSR Demokritos, Athens, GR.
- **Chairman** of the Department of Informatics and telecommunications, University of Athens, GR
- **Head of Division** of Computing Systems and Applications of the Department of Informatics and telecommunications, University of Athens, GR
- **Chairman and member** of several academic councils and delegates, GR, CY, EU
- **Director** of the Computer Centre Facilities of the University of Athens, GR

Teaching

Έχει διδάξει τα τελευταία χρόνια/He has taught the last few years:

1. **Εισαγωγή στην Επιστήμη της Πληροφορικής και των Τηλεπικοινωνιών/Introduction to Computer Science and Telecommunications** (Προπτυχιακό μάθημα κορμού Α! Εξαμήνου/Undergraduate core course 1st semester)
2. **Προηγμένη Αρχιτεκτονική Υπολογιστών/Advanced Computer Architecture** (Μεταπτυχιακό μάθημα /Postgraduate course)
3. **Εισαγωγή στην Κρυπτογραφία/Introduction to Cryptography** (Προπτυχιακό μάθημα επιλογής/Undergraduate elective course)
4. **Θεωρία Πολυπλοκότητας/Complexity Theory** (Προπτυχιακό μάθημα κορμού Α! Εξαμήνου/Undergraduate core course 1st semester)
5. **Αυτόματη Συλλογιστική/Automated Reasoning** (Μεταπτυχιακό μάθημα Τμήματος ΜΙΘΕ/Postgraduate course Dept MHFS)
6. **Υπολογιστές και Υπολογιστική Υψηλών Επιδόσεων (HPC)** (Μεταπτυχιακό μάθημα)
7. **Ιστορία της Πληροφορικής και των Τηλεπικοινωνιών** (Προπτυχιακό μάθημα)

Άλλα μαθήματα που έχει διδάξει στο παρελθόν:

- Λογική Σχεδίαση/Logic Design
- Μικροϋπολογιστές/Microprocessors
- Αρχιτεκτονική Υπολογιστών/Computer Architecture
- Λειτουργικά Συστήματα/Operating Systems
- Λογικός Προγραμματισμός/Logic Programming
- Τεχνητή Νοημοσύνη/Artificial Intelligence
- Θεωρία Παιγνίων/Games Theory
- Έμπειρα Συστήματα/Expert Systems

Scientific activities

1. – Invited speaker in various national and international conferences.
2. – Invited lecturer in various tutorials/workshops.
3. – Chairman of the Steering Committee of the PARLE conferences and member of the Steering Committee of the EURO-PAR conferences.
4. – Member of Organizing Committees of various International Conferences.
5. – Referee in various scientific journals/conferences (IEEE, ACM, etc.)
6. – Consultant and advisor to various organizations (national/international).
7. – Participation in various CEC funded projects (among them project leader of the ESPRIT projects EDS, APPLAUSE, PARACHUTE, and PARROT, all HPCN projects), and GSRT funded projects.

8. – Evaluator/reviewer of various EU funded projects/programs.
9. – National Representative in the policy group of networks EUREKA/Cosine and Person in charge of the Greek Academic Network ARIADNI.
2. – Chairman of Committee of the Selection Committee for Academic Personnel for the Department of Information technology of University of Cyprus (up to 1994).
3. – Evaluator and Reviewer of projects of European Union, Greek GSRT, Ministry of Education.
4. – Main Designer of projects for Office Automation, e-Government Gateway, Data Warehouse and eID for the Cyprus Government (MoF).
5. – Main Designer of the Information System of Environment for the Greek Ministry of Environment, Planning and Public Works.
6. – Main designer of the building, laboratories, human and remaining infrastructure of the Departments of the Faculty of Sciences and Technology of the University of Peloponnese.
7. – Author of the Decennial Planning for the whole University of Peloponnese.
8. – Member of electoral bodies for academic positions for almost all the Greek Universities, as well as for awarding the doctoral diploma.
9. – Member of many Greek committees for drafting specifications, evaluation of offers for a lot of computing Systems of the Greek State and the Wider Public Sector.

R&D interests

A wide range of research interests. Research conducted in the following areas: Computer Architecture, HPCN, Logic design, VLSI design, Artificial Intelligence, Expert Systems, Knowledge Engineering, Logic Programming and Prolog machines, Data and Knowledge bases, Constraints-based programming, Combinatorial Optimization of Scheduling and Planning, Computer Networks, Multimedia and Hypermedia systems, Virtual Reality, Parallel computing, Parallel algorithms, Software Engineering, Systems Analysis and Design, e-Government, Document Management Systems, Affective Adaptive Educational Systems, Adaptive Visualization, Ontologies, Data Mining, Cryptography, Theory of Computation.

R&D Projects (funded ones)

C. Halatsis has participated in the following CEC-funded projects:

- [SPAN](#) of Esprit I (member of the UoA group)
- [EDS](#) of Esprit II (leader for the UoA group)
- [PCA](#) of Esprit II (member of the UoA group)
- [SAFE](#) of Delta (member of the UoA group)
- [OSMOSE1](#) of Esprit I (co-leader of the UoA group)
- [OSMOSE](#) of Esprit II (co-leader of the UoA group)
- [APPLAUSE](#) of Esprit II (leader for the UoA group)
- [GP-MIMD](#) of Esprit II (co-leader of the UoA group)
- [PARACHUTE](#) of Esprit III (leader for the UoA group)
- [MEMOIR](#) of ESPRIT IV (co-leader of the UoA group)
- PARROT of ESPRIT IV (leader of the UoA group and co-technical co-ordinator of the whole project)
- Virtual Museums (leader)

In the the project SPAN of Esprit I the UoA group was engaged in the development of a parallel query processor for relational DB systems.

In the EDS (European Declarative System) project his group has worked together with the ECRC, an industrial research centre common resource of Bull, ICL and Siemens, developing a parallel Prolog environment. In particular his group was responsible for introducing modules, abstract data types, numerical processing capabilities and real-time constructs and for developing a major application in the parallel logic programming language ElipSys, a language that supports various forms of parallelism and constraint programming. The funding for the UoA group was KECU 127 and MDRA 3,5 Matching funds.

In the PCA (Parallel Computing Action) initiative, the group has been funded and has acquired a transputer-based 16-node parallel machine, the Supercluster-16, from Parsytec / Paracom. The machine ran under the Helios operating system, and among other it included the Strand concurrent logic programming language. The machine is connected to our Ethernet LAN, and is used by several members of our department. Our group works on parallel Prolog and parallel relational database retrieval algorithms. The funding for the UoA group was KECU 15.

In the SAFE (Standard Authoring Facility Environment) project has worked on a hypertext-type and object-oriented authoring model for learning. The funding for the UoA group was ECU

In the OSMOSE1 (Open Standard for Multimedia Optical Storage Environments) exploratory action, the group has worked on object-oriented multimedia databases requirements analysis and specification. The funding for the UoA group was ECU

The project OSMOSE (a continuation of OSMOSE-1) was concerned with Multimedia and our role was to develop a multimedia asset management system for the development platform and a query processor for semantic-based multimedia information retrieval for the delivery platform. Outside the scope of these projects, a number of internal projects, related to CAI and RDL, investigated the use of AI and VR in the development of advanced instructional environments. The funding for the UoA group was ECU

APPLAUSE, a continuation of the EDS project, his group was assessing the ECLiPSe language; a parallel logic language with constraints, by developing a multi-agent tourist advisor called MaTourA. This system has been developed in co-operation with ESI, GR, with the intention to provide tourism services via networks. A three-layered communication framework has been developed for the purpose of supporting the communication among the agents in a multi-agent system. ECRC was the prime contractor of this project. The funding for the UoA group was KECU 140,43 and MDRA 10 Matching funds.

In the context of the GP-MIMD project and in co-operation with the Technical University of Athens and the Computer Technology Institute of Patras we acquired a 512-node massively parallel machine for developing and porting various applications. The result of this co-operation has been the creation of the Athens High Performance Computing Laboratory, (AHPCL), a non-profit private company that promotes HPCN applications. The total funding was KECU 600.

In the project PARACHUTE, the UoA, in co-operation with Bull (FR), ILOG (FR) and Olympic Airways (GR), developed a crew management system (crew scheduling and follow-up system). The technology used in this project included object-oriented constraint-based parallel programming. The crew scheduling subsystem covered both the pairing construction and crew assignment (rostering) phases using a C++ constraint programming library, namely ILOG Solver. The funding for the UoA group was KECU 350,67 and MDRA 40 Matching funds.

The MEMOIR project (Managing Enterprise-scale Multimedia using an Open Framework for Information Re-use, EP 22153) demonstrated the applicability and integration of advanced distributed multimedia information systems to support the management of diverse sources of technical information in two large pan-European R&D-based corporations. The demonstration systems developed during the project showed that users could productively access the same source information with very different information requirements via a single underlying information infrastructure. The introduction of such a multimedia information infrastructure will substantially increase the productivity of researchers and other technical information users. In the context of Memoir, the UoA, in co-operation with PAC (UK), Multicosm (UK), IBEX (FR) and two end-user organisations (Glaxo UK, Unichema), has developed intelligent software agents which identify geographically isolated workers who are involved in similar activities, identify relevant information based upon statistical analysis of the content and monitor a variety of dynamic information sources in order to prompt the user with relevant information automatically. The funding for the UoA group was ECU

EP 24960, is the continuation of the PARACHUTE project. The UoA co-operates with ILOG (FR), Lufthansa Systems (D), Olympic Airways (GR) and the University of Paderborn (D) for the improvement of crew rostering quality and performance by applying a parallel approach and by developing on promising results in the combination of operations research techniques and constraint programming. Identification of the optimal mix of techniques and the appropriate

degree of parallelization for the characteristics of different airlines will result in approaches that are adapted to small, medium and large size companies' situations. PARROT follows a preferential bidding policy, it elaborates on a common language, usable trans-nationally, for description of legal, contractual and labour union regulations and rules and, finally, a demonstrator is being built which will be validated and evaluated appropriately. The UoA group is using a direct constraint-programming method and parallelism for solving the rostering scheduling problem. Several search tree algorithms and heuristics are being developed. The funding for the UoA group is KECU 265,50.

Also the group through funding of the IMP for Informatics initiative and that of Structural Funds of the EU Framework Programme has developed a Multimedia laboratory for research, development and services. The lab has all appropriate equipment, to cover all steps of CD-ROM & CD-I publishing (data capture, data editing, authoring / application development, and production), video conferencing, video on demand, Virtual Reality tools and applications.

project concerns the development of a generic Virtual Museum kernel S/W to cover the needs of the various university museums as well as a private museum that participates in the project. More information may be found in the relevant web page. The funding for the UoA group is MDRA 192,3 out of a MDRA 350 total budget.

Publications:

Ph. D. Thesis

C. Halatsis, "Hardware Considerations of Executive and Information Retrieval Systems", Ph.D. Thesis, University of Manchester, Aug. 1971

Publication in scientific journals

1. G. Philokyprou and C. Halatsis, "Floating-Point and Multi-Bit Increment Digital Differential Analyser Structures", Electronics Letters, Oct. 1972, p. 531 – 532, <http://digital-library.theiet.org/content/journals/10>
2. C. Halatsis, G. Philokyprou and D. Maritsas, "Analysis of Block-Organized Buffers for Poisson Input and Periodic Block Output", Int. J. of Systems Science, vol 5, no 1, 1974, <http://dx.doi.org/10.1080/00207727408920074>
3. G. Philokyprou and C. Halatsis, "Electronic Buffer Memories", Int. J. of Electrical Engineering Education, vol 12, pp 25 - 36, 1975, <http://ije.sagepub.com/content/12/1/25.full.pdf+html>
4. C. Halatsis, G. Philokyprou and D. Maritsas, "Designing block-structured bubble-up buffers", Electronic Engineering, April 1976, pp 45-48.
5. G. Philokyprou, C. Halatsis and N. Gaitanis, "On the Problem of Finding d, t, r, and j Type Partition Pairs of a Sequential Machine", IEEE Transactions on Computers, March 1977.
6. C. Halatsis and G. Philokyprou, "Pseudo chaining in Hash Tables", Communications of the ACM 21(7), 554-557, July 1978.
7. C. Halatsis and A. Sokos, "Microprocessor-controlled Elevators", Electronic Engineering, Oct. 1978.
8. C. Halatsis and N. Gaitanis, "Irredundant Normal Forms and Minimal Dependence Sets of a Boolean Function", IEEE Transactions on Computers, Nov. 1978.
9. C. Halatsis and N. Gaitanis, "On the minimization of the Control Store in Microprogrammed Computers", IEEE Transactions on Computers, Dec. 1978.
10. C. Halatsis, M. Sigala and G. Philokyprou, "Polylinear Decomposition of Synchronous Sequential Machines", IEEE Transactions on Computers, Dec. 1978.
11. N. Gaitanis and C. Halatsis, "A new Double-Rank Realization of Sequential Machines", IEEE Transactions on Computers, Dec. 1978.
12. C. Halatsis, M. Sigala and C. Cambakis, "A simple computer-assisted text composition system", Angewandte Informatik, Dec. 1978.

13. C. Halatsis and N. Gaitanis, "Positive Fail - Safe Realization of Synchronous Sequential Machines", IEEE Transactions on Computers, Febr. 1979.
14. N. Gaitanis, C. Halatsis, M. Sigala, "Fail Safe Counters", Journal of Digital Processes, no 5, 1979.
15. A.C. Arvillias, D.G. Maritsas and C. Halatsis, "Microcomputer Implemented Random and Key Stream Generating Mechanisms", Euromicro Journal, 1980.
16. N. Gaitanis and C. Halatsis, "Negative Fail-Safe Sequential Circuits", Electronics Letters, vol 16, no 16, July 1980.
17. A. vanDam, M. Barbacci, C. Halatsis, J. Joosten and M. Letheren, "Simulation of a Horizontal Bit-Slice Processor using the ISPS Architecture Simulation Facility", IEEE Transactions on Computers, July 1981.
18. C. Halatsis, N. Gaitanis and M. Sigala, "Error-Correcting Codes in Binary-Coded Radix-r Arithmetic", IEEE Transactions on Computers, March 1983.
19. N. Gaitanis and C. Halatsis, "A New Design Method for m-out-of-n Totally Self-Checking Checkers", IEEE Transactions on Computers, March 1983.
20. N. Gaitanis and C. Halatsis, "Near-Perfect Codes for Binary Coded Radix-r Arithmetic Units", IEEE Transactions on Computers, May 1983.
21. C. Halatsis, N. Gaitanis and M. Sigala, "Fast and Efficient TSC-Checkers for m-out-of ($2m \pm 1$) codes", IEEE Transactions on Computers, May 1983.
22. A. Hatzopoulos and C. Halatsis, "Microprocessor-based FIR Spectrophotometer", Review of Scientific Instruments, 55(9), Sept. 1984.
23. C. Efstathiou and C. Halatsis, "Efficient Modular Design of m-out-of- $2m$ TSC Checkers, for $m=2^k-1$, $k>2$ ", Electronics Letters, vol 21, no 23, 1985.
24. A. Pombortsis and C. Halatsis, "Performance Analysis of Interconnection Networks of a Modified Model for Synchronous Multiprocessors", Electronics Letters, vol 22, no 4, 1986.
25. A. Pombortsis and C. Halatsis, "Analysis of a Modified Model for Synchronous Multiprocessor Systems", The Journal of Systems and Software, no 6, pp 361-365, 1986.
26. A.M. Paschalis, C. Halatsis and G. Philokyrou, "Concurrently Totally Self-Checking Microprogram Control with Duplication of the Microprogram Sequencer", Euromicro Journal, Microprocessing and Microprogramming, no 20, pp 271-281, 1987.
27. J. Vlachavas and C. Halatsis, "L-Machine: a low cost personal sequential inference machine", The Journal of Systems and Software, 1988.
28. A.M. Paschalis, D. Nikolos and C. Halatsis, "Efficient Modular Design of TSC Checkers for m-out-of- $2m$ codes", IEEE Transactions on Computers, March 1988.
29. A. Pombortsis and C. Halatsis, "Performance of crossbar interconnection networks in the presence of hot spots", IEE Electronics Letters, vol 24, No 3, Febr. 1989.
30. A. Pombortsis and C. Halatsis, "Behavior of circuit-switched Multistage Networks in presence of memory hot spots", IEE Electronics Letters, vol 25, No 13, June 1989.
31. A.M. Paschalis, C. Efstathiou and C. Halatsis, "An Efficient TSC 1/3 Code Checker", IEEE Transactions on Computers, March 1990.
32. P. Stamatopoulos, I. Karali, C. Halatsis, "A Tour Advisory System Using a Logic Programming Approach", Applied Computing Review (ACR), Special Issue on Logic Programming Applications, Sept. 1993.
33. A. Pombortsis and C. Halatsis, "Performance of Circuit-Switched Interconnection Networks Under Non uniform Traffic Patterns", The Journal of Systems and Software, Vol. 20, No 2, Feb. 1993.
34. A. Tsalgatidou, D. Gouskos, C. Halatsis, "Towards the Development of Effective and Flexible Information Systems", Journal of Information Systems, Vol. 1, No 2, 1995.
35. A. Tsalgatidou, C. Halatsis, M. Spiliopouloy, M. Hatzopoulos, "A Multimedia Title Development Environment (MTDE)", Int. Journal of Information Processing & Management, Vol 31, No 1, 1995 (Pergamon Press).

36. Y. Tsiarouhas, A. Paschalids, D. Nikolos, and C. Halatsis, "Robust Test Generation for Transistor Stuck-Open Faults in CMOS Complex Gates", *Int. J. of Electronics*, Vol. 79, No 2, pp 129-142, 1995.
37. E. Karkaletsis, C. Spyropoulos, G. Vouros, C. Halatsis, "Organization and Exploitation of Terminological Knowledge in Software Localization", *TermNet News (TNN), the Journal of International Cooperation in Terminology*, No 48, March 1995.
38. Y. Tsiatouhas, T. Haniotakis, C. Halatsis, A. Arapoyianni, "Design of stuck-open fault testable CMOS complex gates", *Electronics Letters*, Vol. 32, No 4, pp 315-317, 1996.
39. D. Gizopoulos, D. Nikolos, A. Paschalis, C. Halatsis, "C-Testable Modified Booth Multipliers", *J of Electronic Testing: Theory & Applications (JETTA)* Vol. 8, No 3, pp 241-260, June 1996.
40. D. Gizopoulos, A. Paschalis, D. Nikolos, C. Halatsis, "Linear-Testable and C-testable $N_x \times N_y$ Modified Booth Multipliers", *IEE Proc. - Computers & Digital Technique*, Vol. 143, No 1, pp 44-48, Jan 1996.
41. I. Voyiatzis, A. Paschalis, D. Nikolos, C. Halatsis, "An Efficient Built-in Self Test Method for Robust Path Delay Testing", *J of Electronic Testing-Theory & Applications* pp 219-222, June 1996.
42. Y. Tsiatouhas, Th. Haniotakis, D. Nikolos, A. Paschalis and C. Halatsis, "Hierarchical Robust Test Generation for CMOS Circuit Stuck-Open Faults", *International J. of Electronics*, Vol. 82, No 1, pp 45-60, 1997.
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44. D. Gizopoulos, A Paschalis, D. Nikolos, and C. Halatsis, "On robust Two-pattern testing of One-dimensional CMOS Iterative Logic Arrays", *Int. Journal of Electronics*, vol. 86, no 8, pp 967-978, August 1999.
45. I. Vlahavas, P. Kefalas, C. Halatsis, "OASys: An AND/OR parallel logic programming system", *Parallel Computing* 25, pp.321-336, 1999.
46. I. Voyiatzis, A Paschalis, D. Nikolos, and C. Halatsis, "Accumulator-Based BIST Approach for Two-Pattern Testing", *Journal of Electronic Testing, Theory and Applications*, vol. 15, no 3, pp 267- 278, December 1999.
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53. Stergos D. Afantenos, Vangelis Karkaletsis, Panagiotis Stamatopoulos and Constantin Halatsis, "Using synchronic and diachronic relations for summarizing multiple documents describing evolving events", *Journal of Intelligent Information Systems*, March 14, 2007
54. C. Vassilakis, G. Lepouras and C. Halatsis, "A knowledge-based approach for developing multi-channel e-government services", *Electronic Commerce Research and Applications* 6 (2007) 113–124

55. V. Katifori, C. Halatsis, G. Lepouras, C. Vassilakis, E. Giannopoulou, "Ontology Visualization Methods – A survey", *ACM Computing Surveys*, October 2007
56. I. Voyiatzis, A. Paschalis, D. Gizopoulos, C. Halatsis, E. Makri, M. Hatzimihail, "An Input Vector Monitoring Concurrent BIST Architecture Based on a Pre-computed Test Set", *IEEE Transactions on Computers*, Volume 57, Issue 8, Aug. 2008, pp.1012 - 1022.
57. G. Louloudis, B. Gatos, I. Pratikakis & C. Halatsis, "Text line detection in handwritten documents", *Pattern Recognition Journal*, Volume 41, Issue 12 (December 2008), pp. 3758-3772.
58. G. Louloudis, B. Gatos, I. Pratikakis & C. Halatsis, "Text line and word segmentation of handwritten documents", *Pattern Recognition*, vol. 42 (issue 12), pp.3169-3183, 2009
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Contact:

E-mail: halatsis@di.uoa.gr

URL: <http://www.di.uoa.gr/~halatsis>

October 2019