Ge nanocrystal MOSFET memory structure with ordered nanocrystals in the gate dielectric for use in flash memories

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Abstract. This PhD thesis is devoted to the formation of Ge nanocrystals embedded in an insulating matrix (SiO_2) for non-volatile memory applications. Ge nanocrystals present advantages in comparison with Si nanocrystals, related with their better charge retention. Their growth in a 2-D layer within a thin SiO_2 layer in order to fabricate the basic structure of a nanocrystal memory cell was investigated in detail. The second innovation of this thesis is the introduction of lateral ordering in the 2-D layer of Ge nanocrystals, which shows important advantages for the control of their size and position. The ordered Ge nanocrystals were fabricated with electron beam lithography and selective growth in small windows in the SiO_2 layer. The sample structure was studied with transmission electron microscopy, while electrical characterization was used for the investigation of charging phenomena. A Ge nanocrystal non-volatile memory cell with promising characteristics was fabricated and tested.

Keywords: quantum dots, non-volatile memories, Germanium, nanocrystals, electron beam lithography.

1 Introduction

This PhD thesis deals with the investigation of Ge nanocrystal memories [1,2]. The floating gate concept drives the non-volatile memory technology for more than a decade. Flash technology [3-5] serves effectively today's non-volatile memory requirements, but as the requirements grow towards faster, more reliable and higher memory capacity implementations, flash technology fails to follow these requirements. The continuous miniaturization of devices sets a severe limitation to flash devices related to the tunneling oxide thickness, which cannot be scaled down below 6-7nm [6]. One proposal to overcome the scaling down limitation is the replacement of the continuous poly-silicon floating gate of the flash cells with a 2-D discrete nanocrystal layer [7,8]. The introduction of nanocrystals [9] as the charge storage medium permits the use of thinner tunnel oxides. This implementation however sets several issues that have to be addressed, such as nanocrystal fabrication matters like size, density, uniformity and material compatibility with CMOS processes and interpretation of charging, discharging and retention phenomena.

Within this PhD thesis, two issues were addressed in nanocrystal memories. The first issue is the introduction of lateral ordering in the two-dimensional layer of nanocrystals embedded within the gate dielectric of a MOSFET memory cell. The fabrication of ordered arrays of nanocrystals serves the realization of a memory cell with uniform characteristics, since all critical characteristics such as size, uniformity and density are controlled with high precision. The second issue deals with the replacement of the generally used Si nanocrystals by Ge nanocrystals in the floating gate of the MOSFET. In general, the use of Ge nanocrystals in a Si-based non-volatile memory technology [10,11] is believed to increase the retention time of the nanocrystal memory [12]. The increase of the retention time results from the band offset that is introduced between Si and Ge and serves as an additional energy barrier to carriers (especially holes) in their path from the nanocrystals to the Si substrate.

2 Experimental results and discussion

2.1 Electron beam lithography

For the fabrication of ordered Ge dots, electron beam lithography was used. In order to produce patterns with arrays of holes, it was necessary to find a process which would provide the optimum resolution. For the optimization of the lithographic process an extensive lithographic performance study of PMMA took place. This study addressed issues like molecular weight (MW) of PMMA [13] polymers and development schemes in order to find a proper process for the fabrication of the arrays. The study was performed by combining contrast curve measurements, in-situ dissolution studies (DRM) [14] and characterization of high resolution lithographic results using scanning electron microscopy (SEM).

The results showed that a development scheme with isopropanol:water 7:3 (IPA:H$_2$O) along with a 996k MW PMMA demonstrates superior lithographic performance compared with the rest of development schemes studied i.e. methyl isobutyl ketone 1:3 (MIBK:IPA 1:3) [15]. With this lithographic process, arrays of holes were patterned on PMMA resist and after dose and development time optimization, holes of a diameter of 45nm with a 100nm pitch were optimally produced. The dose used was in the range of 2-2.5fC per hole and development was performed in IPA:H$_2$O 7:3 in an ultrasonic bath for 30s. In fig. 1 a Scanning Electron Microscopy (SEM) image of the lithographic pattern is illustrated.
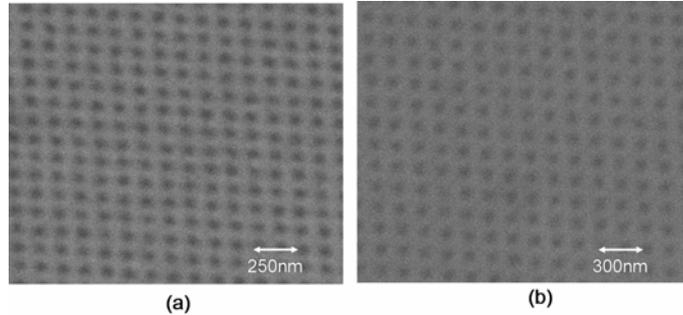
Fig. 1. SEM micrograph of ordered arrays of holes in PMMA. In (a) the pitch was 125nm and in (b) 150nm.

2.2 Ordered Ge dots fabrication

For the fabrication of ordered Ge nanocrystals, electron beam lithography was used for the realization of a basic pattern which consisted of arrays of holes patterned in a 70nm thick PMMA resist layer. With the arrays of holes serving as the basic pattern, several different processes were deployed in order to fabricate arrays of ordered Ge nanocrystals as illustrated in the process flow charts of fig. 2. One goal was to examine how Ge can be epitaxialy grown on confined Si surfaces (nucleation sites). Nucleation sites were fabricated by transferring the pattern of holes arrays from PMMA to the SiO_2 layer by etching. The SiO_2 layer was 3.5nm thick and was grown thermally (dry oxidation of Si at 850°C for 8min) on Si substrates. The selective growth of Ge was investigated in plain SiO_2 windows or in V-grooves in Si [16,17]. V-grooves were fabricated by anisotropic etching of Si, with the patterned SiO_2 serving as a mask. For the dot growth, a Low Pressure Chemical Vapor Deposition (LPCVD) system was used.
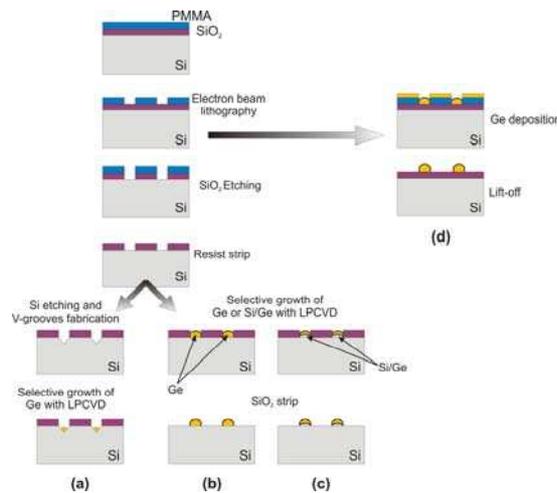

Fig. 2. Process flow chart for the fabrication of ordered Ge nanocrystals. (a) In V-grooves, (b) and (c) in plain windows in SiO_2 and (d) with lift-off.

The results show that the growth of Ge depends on window size (see fig. 3) [16,17]. If the window size is smaller than 270nm, one dot per window is obtained, otherwise for larger window areas we have more than one dot per window. With such a process it was possible to obtain arrays of Ge dots or Si/Ge hetero-epitaxial double dots which all followed the initial pattern (plain Si window or V-groove). While this approach produced very good results regarding uniformity and growth control, the isolation of the Ge dots directly grown on the Si substrate was proved a difficult task since Ge tended to diffuse towards the interface with Si faster than oxygen. Isolation of Ge dots was investigated by oxidizing the structure.
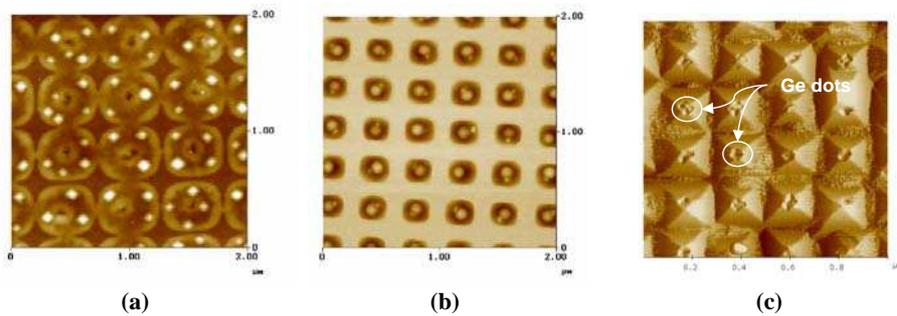

| (a) | (b) | (c) |

Fig. 3. AFM images of Ge islands grown in Si V-grooves. In (a) 3 to 4 dots were grown per V-groove (500nm V-groove opening). In (b) the V- grooves were smaller (270nm) and one large dot was formed per groove, with one smaller dot attached to it in some cases. In (c) we see an inverted image of a V-groove, 200nm large , where one dot per groove is identified.

The production of a good quality tunnel oxide underneath the dot requires good control of the oxidation. With this in mind, a lift-off process was developed and ordered Ge dots were fabricated on a pre-fabricated SiO_2 layer. The lithographic pattern of holes arrays was used, Ge was deposited on the patterned PMMA layer and after lift-off, ordered Ge dots on the tunneling SiO_2 layer were formed. By covering the samples with SiO_2, MOS capacitor structures were fabricated and tested by electrical measurements. It was shown that positive carriers (holes) can be injected from the Si substrate to the dots, thus charging the Ge layer. This effect was observed only in the areas where Ge dot arrays were fabricated and not in structures without Ge dots, showing that the hole trapping is related to the presence of Ge dots as can be seen in fig. 5.
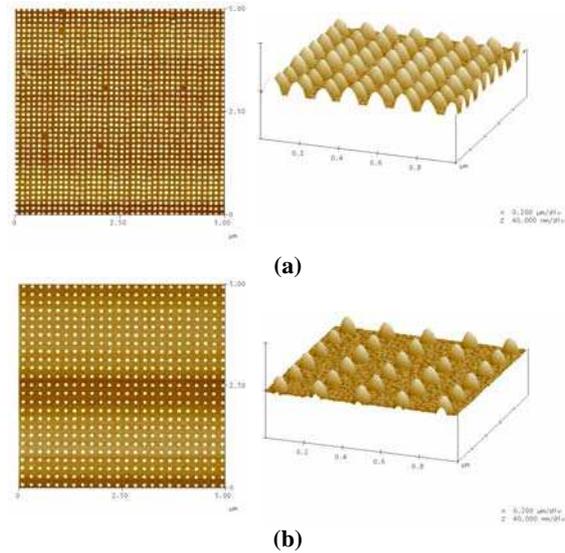
(a)

(b)

Fig. 4. AFM plan views and corresponding 3-D expanded images of arrays of Ge/Si hetero-nanocrystals grown on arrays of holes in SiO$_2$. The lithography pitch in (a) was 150 nm while in (b) it was 200 nm. The mean dot size in (a) was 95 nm, while in (b) it was 90 nm.
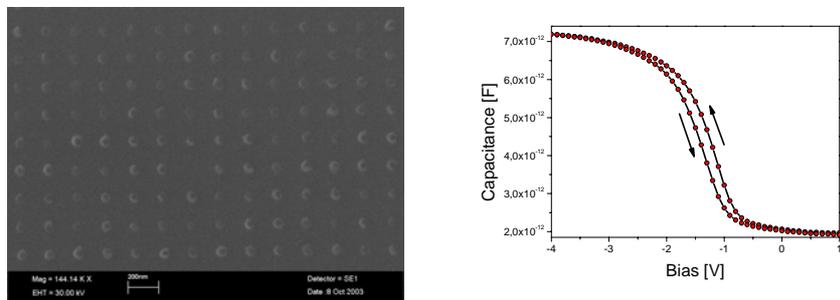

Fig. 5. (a) SEM image of Ge dots grown on tunneling SiO$_2$ layer. (b) Capacitance-Voltage measurements of capacitors containing arrays of Ge dots. A clear hysteresis effect is present.

2.3 Ge dot formation within SiO$_2$ – Electrical characterization

The formation of randomly distributed Ge nanocrystals [18,19] in a SiO$_2$ matrix was studied by combining Ge deposition on a 3.5nm thick SiO$_2$ layer and covering with a TEOS or sputtered SiO$_2$ layer serving as the control oxide of the structure. The main issue was to find a process which could lead to the formation of isolated Ge nanocrystals in SiO$_2$. In all experiments, oxidized Si samples were used on which Ge

was deposited within a range of thicknesses from 1 to 2.3nm. For the deposition, three different techniques were used: Molecular Beam Epitaxy (MBE), e-gun evaporation and sputtering. In MBE samples, in-situ annealing was performed after Ge deposition in order to form Ge nanocrystals. In the rest of techniques, rapid thermal annealing processes took place after the control SiO_2 layer was deposited.

Structural characterization of the fabricated samples was performed by Transmission Electron Microscopy (TEM) both in cross section and plan view imaging. Information about the effect of the thickness of the material deposited and thermal annealing processes on the Ge dots layer formation was deduced from these experiments. The conditions that were studied for both initial Ge thickness and thermal annealing did not lead to a clear evidence of separate Ge nanocrystal formation as can be seen in fig. 6. The observed dots were rather amorphous in that case. It was clear though that the formation of Ge nanocrystals is related to the thickness of the initial deposited Ge film and thermal annealing ambient and temperature.
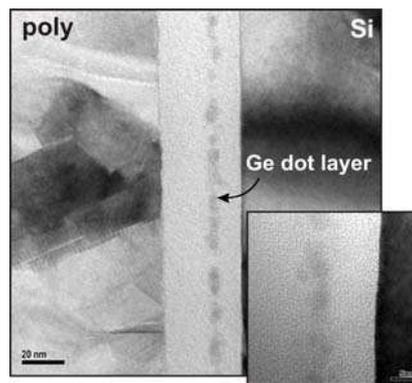

Fig. 6. Cross sectional TEM image of the Ge layer within SiO_2

Electrical characterization of both MOS capacitors and transistors (memory cells) was performed, in order to study the behavior of the structures regarding memory effects. In MBE samples (1nm Ge) a large positive shift (~3V) indicating electron injection from the substrate to the Ge layer was observed. Nevertheless, discharge of the structure was difficult. This was attributed to the fact that electrons occupy a large density of deep traps in the energy gap. In the case of e-gun evaporation, where 2.3nm of Ge were initially deposited, better results were obtained and a working memory cell was successfully fabricated. The cell could perform write-erase cycles, as in normal operation of a memory cell and with pulses of ±8V for 1s, a 130mV memory window was obtained as can be seen in fig. 7.
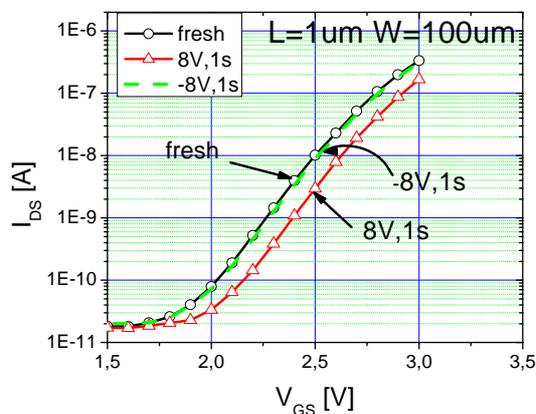
Fig. 7. Drain-Source current vs Gate-Source bias characteristic of a Ge nanocrystal memory cell after charging with ±8V, 1s write-erase pulses .

3   Conclusion

With this PhD thesis the technology of fabricating arrays of ordered and uniform Ge nanocrystals within the gate dielectric of a MOSFET for use in nanocrystal non-volatile memories was developed. The top-down technique of electron beam lithography was used, combined with successive process steps for Ge dots growth by UHV-LPCVD. It was shown that the number of dots grown inside each SiO_2 window depends on the size of the window and below 270nm one dot per window can be grown. MOS structures with ordered Ge dots within SiO_2 were also fabricated and tested electrically. Formation mechanisms of Ge nanocrystals within SiO_2 were addressed. A Ge nanocrystal memory cell with promising characteristics was developed.

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