Testing and Performance Calibration Techniques for Integrated RF Circuits

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Abstract. In this dissertation, a unified approach is proposed for the testing and calibration procedures of integrated RF circuits, that exploits a common set of optimally selected observables. In order to address the problem of accessibility to these observables, a built-in measurement technique is presented, while a method to minimize the uncertainty introduced in the measurement system itself is described, as well. By the application of selection algorithms, the number of observables is reduced through an optimization procedure, leading to test cost savings due to the reduction of test conduction complexity and time.

Keywords: Defect Detection, Integrated Circuits, Mixers, Performance Calibration, Wireless Transceivers

1 Introduction

Specifications of analog integrated circuits (ICs), especially radio frequency (RF) circuits, have become increasingly strict as their applications tend to be more complex and demanding. To meet these specifications, an often painstaking and time-consuming series of repetitive design cycles has to be undertaken which, however, cannot guarantee that all fabricated circuit instances are acceptable in terms of their expected performance.

In order to assure reliability, each fabricated IC should be subject to a testing procedure aiming to ascertain that the circuit is functional and, furthermore, compliant to its specifications. In the conventional RF IC testing approach, automatic test equipment (ATE) is used to sequentially measure the performance characteristics of a circuit under test (CUT). Although these measurements are simple, they require a variety of test resources which, together with the long test application times, increase the total manufacturing cost. In many cases testing cost turns to be unacceptable, tending to be comparable to the rest manufacturing cost [1]. To overcome the inabilities of conventional testing, alternative low-cost techniques have been proposed, the most notable being defect-oriented testing (DOT) and 'alternate' test.

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Defect-oriented testing, or structural testing, follows the assumption that most or all defect mechanisms that commonly lead to malfunctioning circuits manifest themselves in more fundamental observables than the specifications, thus simplifying the test procedure and also reducing cost. DOT efficiency is primarily determined by the defect detection capability obtained by the selected observables and the cost for their stimulation and measurement. On the other hand, the objective of the alternate test methodology [2] is to find a suitable test stimulus and to accurately predict the circuit's performance from the corresponding alternate test response. Appropriate selection of the set of observables which compose the test response crucially determines prediction accuracy; however, test simplicity is often compromised leading to increased cost [3].

As an outcome of the test procedure, a portion of the tested circuits is, unavoidably, rejected: Catastrophic failures due to physical limitations, together with the variability of a large number of parameters affecting the IC production processes, constitute the problem of yield loss. Although process variations do not necessarily lead to a defective circuit in terms of functionality, a large amount of manufactured circuits might, however, fail to comply with their performance specifications, leading to an increased yield loss which turns to be significant in nanometer technologies [4, 5].

Several calibration methods have been proposed, which address the issue of increased parametric yield loss by compensating for parametric variations using on-chip resources [6, 7]. A critical issue to be addressed in the calibration procedure is the appropriate selection of the specific circuit's state at which performance is restored to acceptable levels.

A key problem in both RF IC testing and calibration is that it is not always possible for the ATE to have direct access to all or even part of the internal signals of an IC, especially in system-on-chip (SoC) or system-in-package (SiP) designs. Although some internal signals can be made available to the external tester, frequency limitations due to the lower speed of the I/O interface may not permit their direct observation.

A unified low-cost approach for the testing and calibration procedures of integrated RF circuits is proposed in this dissertation, which exploits a set of optimally selected observables. The exploitation of these observables enables both defect detection and prediction of the circuit's performance, allowing the examination of compliance with the specifications and performance calibration, as well. A combination of the DOT and alternate test methodologies is used to maximize fault coverage, while both alternate test accuracy and calibration efficiency are increased by the exploitation of the adjustable features of the circuits under consideration. In order to address the problem of accessibility to test observables, a built-in technique is proposed, while a method to minimize the uncertainty introduced in the measurement system itself is also described. The application of selection algorithms is explored, aiming to reduce the number of test observables through an optimization procedure that leads to test cost savings due to the reduction of the test conduction complexity and time.

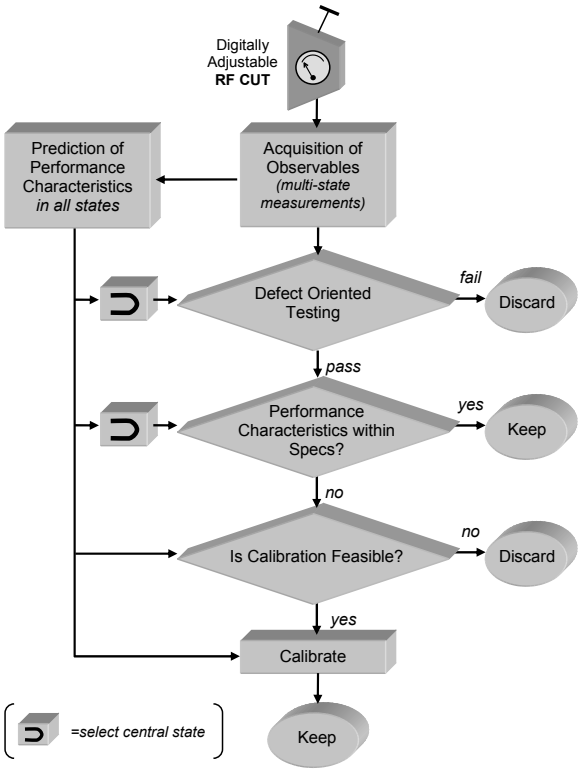

Fig. 1. Testing and calibration flow

The efficiency of the proposed techniques is validated by their application to a typical RF mixer designed in a 0.18m CMOS technology. Simulation results are obtained and assessed, while comparison with similar conventional methodologies is also provided.

2 A Test and Calibration Strategy for Adjustable RF Circuits

2.1 Methodology

We consider adjustable RF circuits, that are designed such as to be able to operate in several discrete states, thus providing the capability to vary their performance characteristics (PCs) around their post-fabrication values. This functionality is obtained by the use of an adjustable element, the value of which is related to the circuit's performance characteristics under consideration.

The proposed test and calibration methodology is illustrated in Fig. 1 and synopsized as follows. First, the adjustable RF CUT is measured in various states to obtain a specific set of test observables according to the alternate

test approach. Then, its performance characteristics are predicted for all states of operation using pre-developed regression models [8]. The set of measured observables, together with the predicted performance characteristics, are used for defect detection, while the predicted performance characteristics in a single state (the central state) of operation are sufficient for defect detection, as shown in [9]. Defect-free circuits are examined to determine if their predicted performance characteristics in the central state comply with the specifications. The predicted performance characteristics in the remaining states are used to explore the ability to calibrate each circuit found to be non-compliant. Finally, circuits for which their predicted performance characteristics in at least one state are compliant with the specifications are calibrated exploiting the existing adjustable element.

Testing Procedure The first step towards defect detection is the derivation of the expected range of values, due to process variations and device mismatches, for each individual observable as well as for each predicted performance characteristic. The derivation of these ranges, for which we adopt the term "variation bands", assumes defect-free circuits.

To maximize defect detection efficiency, we may consider to extend the initial set of observables ($\boldsymbol{O}$) to a superset of extended observables ($\boldsymbol{E}$), whose elements represent either an initial observable or a simple linear combination of these observables. The latter can be determined by specifying correlations between elements of $\boldsymbol{O}$, either through empirical observation or via principal component analysis (PCA). The derivation of the corresponding variation bands is performed by statistical analysis on a sample of either actual or Monte-Carlo simulated instances, as explained in detail in [9]. Figure 2(a) summarizes the overall procedure followed for the derivation of the variation bands.

Defect detection is carried out after the extended observables are calculated, as illustrated in Fig. 2(b), while the predicted performance characteristics for the circuit's central state of operation are also considered. Defect detection is accomplished according to the following rule: If at least one of the extended observables (in a DOT sense) or at least one of the PCs (in an alternate test sense) fails to fall within its corresponding variation band, the CUT is classified as defective and discarded, otherwise it is considered to be free of defects. If the latter is true, a calibration procedure is initiated in the case where predicted PCs in the central state do not comply with the specifications, in order to reduce parametric yield loss.

Calibration Procedure The calibration procedure determines the circuit's state of operation for which all predicted performance characteristics comply with their specifications. This is possible by the exploitation of the regression models that have been constructed for all PCs and all states of the circuit's operation, according to the principle described in Fig. 3. In this figure, an example of a correctable circuit is shown, since for the state *S2* all predicted PCs meet the specifications simultaneously. On the contrary, for the uncorrectable circuit

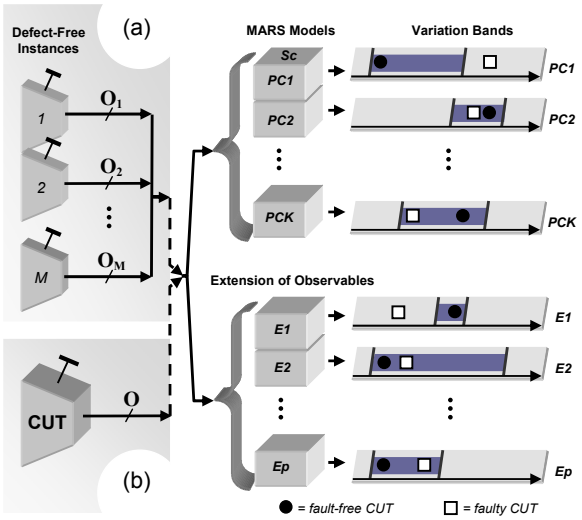

Fig. 2. Procedure for (a) the derivation of the variation bands (shaded areas) and (b) defect detection

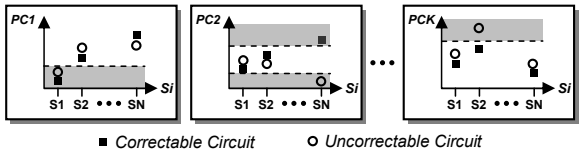

Fig. 3. Calibration principle. (Shaded areas indicate non-compliant performance characteristic ranges, while S_i (i=1,2, ... ,N) correspond to the circuit's states of operation)

instance shown in the same figure, no state exists for which all predicted PCs fall inside their acceptable ranges.

2.2 Evaluation

The effectiveness of the proposed methodology has been evaluated by simulations on a typical RF mixer. The mixer under consideration, presented in Fig. 4, is designed in the 0.18μm Mixed-Signal/RF CMOS technology of UMC (Vdd=3.3V) with an intermediate frequency (IF) of 150MHz. A digitally controllable resistor R_{var} in the mixer's bias circuitry has been used as the adjustable element, by which the mixer's current is controlled and states of the circuit's operation are provided, as summarized in Table 1 where the values of each PC of interest – namely, gain (G), 1dB compression point (1dB CP) and input referred 3rd order intercept point (IP3) – are also presented for each state.

In this case study, we adopt the use of the local oscillator's (LO) signal as the test stimulus at the RF inputs of the mixer [3, 7, 10]. The self-mixing of the LO signal forces the mixer to operate in homodyne (zero IF) mode, generating

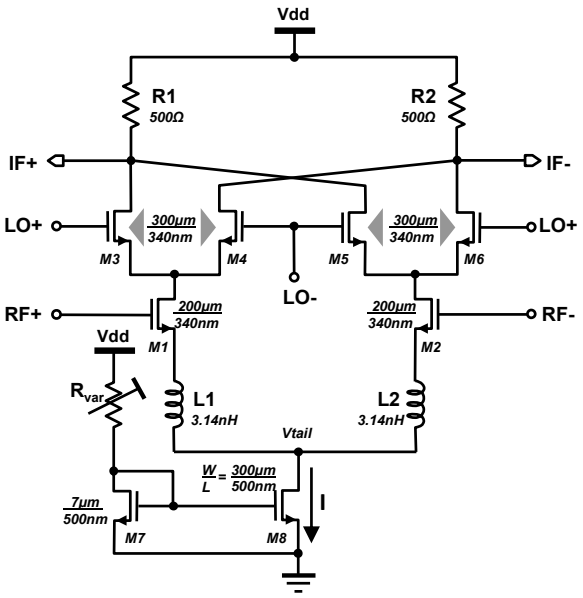

Fig. 4. The adjustable RF mixer under consideration

Table 1. RF mixer states of operation

State ID *(Si)*	G *(dB)*	1dB CP *(dBm)*	IP3 *(dBm)*	I *(mA)*
S1	3.68	-1.77	7.52	3.63
S2	4.03	-0.92	8.60	4.08
*S3**	*4.39*	*-0.19*	*9.73*	*4.67*
S4	4.72	0.62	10.88	5.46
S5	4.85	0.85	10.72	6.58

* central state (S_c=*S3*)

DC voltage levels at its "IF" outputs. The aforementioned DC levels (IF_+, IF_-) are used as the main observables, together with the DC voltage component of the mixer's tail voltage (denoted as V_{tail} in Fig. 4).

It has been proven that prediction accuracy improves significantly if the voltage observables are obtained from more than one of the mixer's states. Specifically, only two states are enough to provide very high prediction accuracy [11], namely the central state (*Sc=S3*) and the maximum tail current state (*S5*). Furthermore, observables are extended such as to include the differential mixer output voltage in test mode, since this inclusion increases DOT effectiveness [9,10].

Defect Detection All possible defects (38 opens, 43 shorts, 13 bridgings) have been simulated in the presence of process variations and device mismatches, set-

Table 2. Defect detection probability results

Type of Defect	Defect Detection Probability (%)		
	Defect-Oriented ***(E)***	*Alternate* ***(PC)***	*Combined* ***(E, PC)***
Shorts	78.58	99.14	100
Opens	100	89.26	100
Bridgings	100	70.15	100
Overall	*90.20*	*91.14*	***100***

ting the mixer in both selected states. Defect detection probabilities have been calculated and the results are summarized in Table 2, where columns labeled "Defect-Oriented" and "Alternate" correspond to the probabilities obtained by the extended observables ($\boldsymbol{E}$) and the predicted performance characteristics ($\boldsymbol{PC}$), respectively, while "Combined" indicates the result obtained by using both the DOT and the alternate test approaches. According to these results, all defects can be detected successfully since a detection probability of 100% is provided. This ensures that all mixer instances entering the succeeding calibration phase are free of defects and, hence, candidate for calibration.

Calibration It is assumed that specifications for the mixer under consideration require: 4dB$\leq$G$\leq$5dB, 1dB CP$\geq$–0.5dBm and IP3$\geq$9dBm. It has been observed that 48.57% of the instances involved in the calibration procedure are found to comply with the specifications before calibration. After applying the proposed calibration technique, the amount of compliant mixer instances corresponds to 88.57%, which indicates a +82.35% relative yield improvement. Similar improvement has also been reported for different specification requirements [11].

3 A Built-In Voltage Measurement Technique for the Calibration of RF Mixers

The proposed built-in technique addresses the problem of accessibility to the alternate test response signals that are necessary for the conduction of an RF mixer calibration procedure. The procedure described in the previous section is adopted.

3.1 Design and Implementation

By utilizing a ring-type voltage-controlled oscillator (VCO) and a counter, a low-cost time-based analog to digital converter (ADC) is constructed which is used as a voltage acquisition circuit (VAC, shown in Fig 5) that provides digital readings for the alternate test voltage observables.

A setup that allows the application of the test stimulus and the connection of the VAC to the appropriate mixer node for DC voltage acquisition follows the

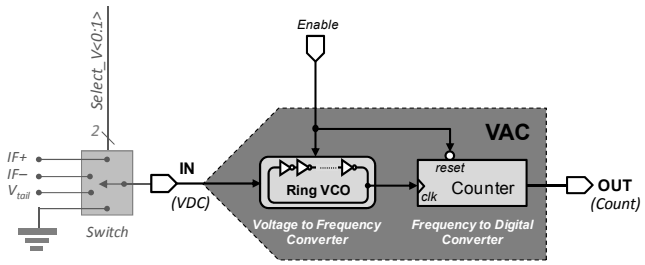

Fig. 5. Voltage acquisition circuit (VAC)

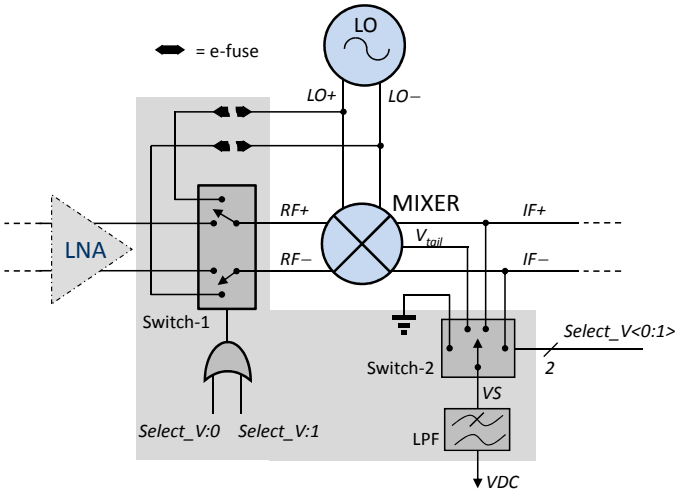

Fig. 6. RF mixer design modifications (shaded area)

scheme presented in Fig. 6, which illustrates the case of a differential RF mixer in a receiver. However, the proposed setup can be easily extended to cover both mixers in transceiver circuits, following the shared resource approach presented in [12]. In order to provide a built-in solution, an analog switch (Switch-1) disconnects the mixer's differential input from the low noise amplifier (LNA) and connects it to the LO. A second analog switch (Switch-2), as presented in Fig. 6, is used to select a voltage observable among IF+, IF– and V_{tail}, one at a time and also provides the ground level required for the correction of the VAC readings, as it is explained in [13]. A common RC low-pass filter (LPF) is connected to the output of the second switch to reject any remaining high-order frequency components and to provide a DC voltage signal (VDC).

Aiming to avoid the influence of the LO signal on the RF signal path in the normal mode of operation, through the first switch, low cost electrical fuses (e-fuses) or laser-cut fuses can be optionally exploited to eliminate the LO-RF test path after the completion of the measurements procedure.

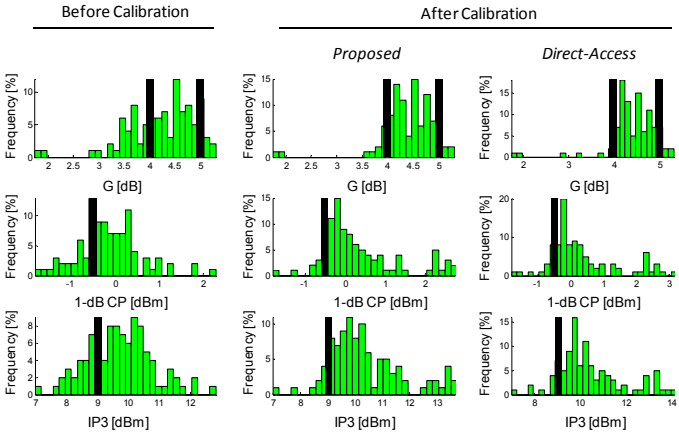

Fig. 7. Distributions of performance characteristics, before and after calibration

3.2 Evaluation

To assess the efficiency of the calibration procedure, as conducted using the proposed measurement technique, an evaluation set consisting of extremely perturbed defect-free mixer instances was generated using Monte Carlo simulations. Specification requirements for the mixer under consideration were defined as follows: 4dB$\leq$G$\leq$5dB, 1 dB CP$\geq$0.5dBm and IP3$\geq$9dBm.

The reported efficiency of the calibration procedure is illustrated in Fig. 7 where the distributions of performance characteristics before and after calibration are presented both for the proposed technique and the direct-access case, for the sake of comparison. Bold vertical lines indicate the margins of acceptable performance as set by the specifications. For the mixer's specifications under consideration, 42% of the instances involved in the calibration procedure are found to comply with the specifications before calibration. After the application of the proposed calibration procedure, the amount of compliant mixer instances corresponds to 75%, which indicates a +78.6% yield improvement, while for the direct-access approach a slightly higher yield (77%) is reported, which corresponds to a difference of only 2.5%.

4 Adjustable RF Mixers' Alternate Test Efficiency Optimization by the Reduction of Test Observables

Alternate tests for adjustable RF mixers are considered, where the alternate test response (ATR) consists of DC voltage levels while the mixer operates in homodyne mode, as presented in the previous sections. Selection techniques are proposed to determine the set of optimum test response observables. This is a subset of all available observables, obtained from all states, which is selected through specific optimization procedures in order to minimize a certain cost criterion that incorporates both test accuracy and complexity.

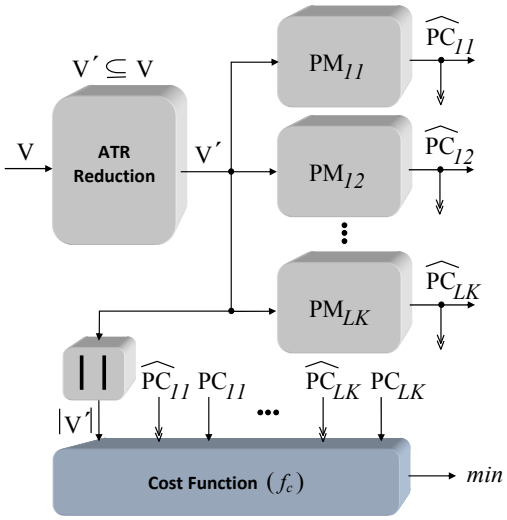

Fig. 8. Principle of ATR reduction (global approach)

4.1 Methodology

The proposed methodology aims to reduce the number of observables that are used as inputs to the predictive models, without a significant compromise of the corresponding alternate test accuracy. It has been found [14] that a 'global' approach is more efficient compared to its 'local' counterpart. Instead of the selection of an optimum subset of observables per individual model, the global ATR reduction approach attempts to minimize a cost function using a single common subset V' of the full set of potential model inputs (V) for all predictive models (PM_{lj}), as shown in Fig. 8. Actual performance characteristic values (PC_{lj}) and their predicted counterparts ($\widehat{PC_{lj}}$) corresponding to all predictive models are used as inputs to the cost function in order to provide a global measure of the corresponding accuracy, while the cardinality $|V'|$ of the common reduced subset of observables is used as a measure of test complexity.

Since an exhaustive examination of all subsets V'_{lj} of V in order to find the optimum subset which leads to a cost function minimum would require a rather large number of predictive model construction and evaluation trials, low complexity selection algorithms are adopted, namely sequential forward selection (SFS) and sequential backward selection (SBS). Furthermore, the inherent input selection capabilities of the regression algorithm (i.e., the MARS algorithm [8]) are explored, as well.

4.2 Evaluation

By the application of the proposed methodology, conduction of alternate tests on the adjustable RF mixer presented in the previous sections has led to the results

Table 3. Prediction error vs. test complexity for responses obtained by different global observable selection methods

SFS

error (e)	<1%	<1.2%	1.6%
reduction of observables	5/15 (33%)	7/15 (47%)	10/15 (67%)
accuracy degradation *(with respect to minimum achievable error)*	4.5%	28.1%	79.8%

SBS

error (e)	<1%	<1.1%	1.3%
reduction of observables	6/15 (40%)	7/15 (47%)	9/15 (60%)
accuracy degradation *(with respect to minimum achievable error)*	5.2%	19.7%	45.5%

MARS

error (e)	<1%	<1.3%	<1.6%
reduction of observables	6/15 (40%)	9/15 (60%)	11/15 (73%)
accuracy degradation *(with respect to minimum achievable error)*	6.7%	38.2%	76.4%

shown in Table 3. These results indicate that several cases exist for which a significant reduction of observables is associated to only a small accuracy degradation with respect to the minimum achievable error. For example, a 33% reduction of observables is followed by an accuracy degradation of only 4.5% in the SFS case presented in Table 3. However, even when a significant relative accuracy degradation is reported, a relatively low corresponding absolute variation is observed (i.e. an increase of 0.6% in the absolute error corresponds to a 76.4% relative accuracy degradation).

5 Conclusions

In this dissertation we have shown that testing and calibration procedures for integrated RF circuits can be viewed in a common framework, leading to reliable low-cost solutions. High defect coverage and significant reduction in parametric yield loss are reported, while the prediction of the performance characteristics is significantly improved by exploiting the adjustable features of the RF circuit under test.

It has also been shown that it is feasible to conduct highly efficient calibration procedures on integrated RF circuits, even when the measured alternate test response consists of voltage components which appear at internal nodes, overcoming the accessibility limitations met in embedded systems. A significant reduction in parametric yield loss is reported for the proposed built-in techniques,

which is very close to that achieved by direct measurements of the alternate test response.

Finally, it has been proven that alternate test complexity or, equivalently, cost can be further reduced by the selection of the optimal test response, with a negligible degradation of accuracy.

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